AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 8, line 16 and ending on page 9, line 2, with the following amended paragraph:

The various aspects of the invention will now be described in greater detail with reference to FIG. 2, which is a block diagram of a system that employs a BER estimator that operates in accordance with the invention. At a transmitter, data to be transmitted is supplied to error detection, coding and interleaving logic 201, which generates error detect bits for each block of data to be transmitted, and then generates interleaved FEC bits from the information and error detect bits. These bits are then imposed onto a signal (e.g., by means of binary phase shift keying, BPSK) that is propagated through a channel 203. At a receiver, the received signal 205 is supplied to decoding, deinterleaving and error detect logic 207, which performs deinterleaving and error correction decoding as described above to generate a stream of decoded bits ("Received Data") 209. The error correction decoding technique can include the use of Viterbi processing. The decoded bits 209 are supplied to other circuitry (not shown) in the receiver which uses them for their intended purpose (e.g., generating a loudspeaker signal in a mobile communication device). The decoding, deinterleaving and error detect logic 207 further generates an error detect signal 211 that indicates whether the decoded bits 209 include at least one erroneous bit. The generation of the error detect signal 211 may, for example, be based on a comparison of receiver-generated CRC bits with received CRC bits that had been added to the information bits by the transmitter prior to error correction coding and interleaving. If the two sets do not match, then an error is indicated.